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Harmonic Mitigation using Seven-Level Shunt Active Power Filter for High-Power Drive Systems

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Abstract:
In high-power adjustable-speed motor drives, such asthose used in electric ship propulsion systems, active filters provide a viable solution to mitigating harmonic related issues caused by diode or thyristor rectifier front-ends. To handle the large com-pensation currents and provide better thermal management, two or more paralleled semiconductor switching devices can be used. In this paper, a novel topology is proposed where two active filter inverters are connected with tapped reactors to share the compen-sation currents. The proposed active filter topology can also pro-duce seven voltage levels, which significantly reduces the switching current ripple and the size of passive components. Based on the joint redundant state selection strategy, a current balancing algo-rithm is proposed to keep the reactor magnetizing current to a minimum. It is shown through simulation that the proposed active filter can achieve high overall system performance. The system is also implemented on a real-time digital simulator to further verify its effectiveness.
Key Words: power electronics , Adjustable-Speed Drive, Active filters, harmonic analysis, Power Measurements.

I. Introduction:

Adjustable Speed-motor Drives (ASDs) have found extensive application in a variety of high-power systems. One example is the electric propulsion system used in modern naval ships, the power ratings of which can be tens of megawatts. Typically, the front-ends of such ASDs employ a diode or a thyristor rectifier. In spite of their simple control and robust operation, these devices can generate voltage and current harmonics that might affect the operation of other devices in the same ac system. Conventionally, passive LC filters are used to mitigate harmonic-related problems.

However, due to their large size and inflexibility, passive filters are gradually being replaced by active filters that utilize power electronic inverters to provide compensation for harmonics. Among various active filter configurations, the shunt active filter systems have a number of advantages and constitute the optimal harmonic filtering solution for ASD rectifier front-ends. In general, the ratings of shunt active filters are based on the rms compensating current and the rms filter terminal voltage. For high-power applications such as ship propulsion systems, the large compensation current often requires parallel operation of two or more switching devices or active filters.

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In recent years, multilevel converters have shown some significant advantages over traditional two-level converters, especially for high-power and high-voltage applications. In addition to their superior output voltage quality, they can also reduce voltage stress across switching devices. Since the output voltages have multiple levels, lower dv/dtis achieved, which greatly alleviates electromagnetic interference problems due to high-frequency switching. Over the years, most research work has focused on converters with three to five voltage levels, although topologies with very high number of voltage levels were also proposed. In general, the more voltage levels a converter has the less harmonic and better power quality it provides. However, the increase in converter complexity and number of switching devices is a major concern for a multilevel converter.

It has been shown that although more voltage levels generally mean lower total harmonic distortion (THD), the gain in THD is marginal for converters with more than seven levels. This paper

presents a shunt active filter configuration that uses tapped reactors for harmonic current sharing. It reduces current stress of the switching devices by distributing the compensation current between two parallel legs of an H-bridge topology. It also reduces voltage stress across the switches by utilizing a conventional three-level flying capacitor topology. Overall, the configuration is capable of producing seven distinct voltage levels, and thus, greatly reduces switching ripple in the compensating currents.

The concept of the configuration was introduced in a previous conference publication. Herein, more detail of the topology and control are presented. Additional simulation studies are also carried out as well as corresponding studies using a real-time digital simulator (RTDS). The studies herein are also conducted on a full motor drive system, whereas in the previous work, the system was supplying a resistive load.

The rest of this paper is organized as follows. The active filter topology is briefly described in Section II. The control algorithm of the active filter is discussed in Section III. Simulation results are presented in Section IV to evaluate the proposed configuration and control. In addition, the system is implemented on RTDS hardware to further validate the proposed active filter, and the results are also presented in Section V. Finally, the conclusions are given in Section VI.

II. Active Filter:

An active filter is a type of analogelectronic filter, distinguished by the use of one or more active components i.e. voltage amplifiers or buffer amplifiers. Typically this will be a vacuum tube, or solid-state (transistor or operational amplifier).

Active filters have three main advantages over passive filters:

- Inductors can be avoided. Passive filters without inductors cannot obtain a high Q (low damping), but with them are often large and expensive (at low frequencies), may have significant internal resistance, and may pick up surrounding electromagnetic signals.
- The shape of the response, the Q (Quality factor), and the tuned frequency can often be set easily by varying resistors, in some filters one parameter can be adjusted without affecting the others. Variable inductances for low frequency filters are not practical.
- The amplifier powering the filter can be used to buffer the filter from the electronic components it drives or is fed from, variations in which could otherwise significantly affect the shape of the frequency response.

A. Tapped Reactor Model

Unlike the center-tapped inter phase reactor [9]–[12], the re-actor in the proposed topology has a tap terminal at its one-third position, as shown in Fig. 2. For the convenience of analysis, the reactor can be divided into two parts. In Fig. 2, part one, denoted as L_1 , consists of the portion from terminal $x1$ to the tap and has a number of turns $N_1 = N$; part two, denoted as L_2, consists of the portion from the tap to terminal $x2$and hasa number of turns $N_2 = 2N$. Terminals $x1$ and $x2$ are defined as the input terminals while the tap terminal is defined as the output terminal x

S_a	v_{a1}	v_{a2}	v_{ax}
0	0	0	0
1	0	$v_{dc}/2$	$v_{dc}/6$
2	$v_{dc}/2$	0	$v_{dc}/3$
2'	0	v_{dc}	$v_{dc}/3$
3	$v_{dc}/2$	$v_{dc}/2$	$v_{dc}/2$
4	$v_{dc}/2$	v_{dc}	$2v_{dc}/3$
4'	v_{dc}	0	$2v_{dc}/3$
5	v_{dc}	$v_{dc}/2$	$5v_{dc}/6$
6	v_{dc}	v_{dc}	v_{dc}

TABLE I
ACTIVE FILTER LINE-TO-GROUND VOLTAGES

To derive the relationship between the input voltages and the output voltage, an ideal model of the tapped reactor is considered first in which there are no losses and no leakage flux. The following assumptions are made.

1) The core of the reactor is highly permeable in a sense that it requires vanishingly small magnetomotive force to set up the flux.
2) The core does not exhibit any eddy current or hysteresis loss.
3) All the flux is confined in the core, so there is no leakage flux.
4) The resistance of the reactor is negligible.

Suppose that voltages v_{x1} and v_{x2} , with respect to a common ground, are applied to the input terminals $x1$ and $x2$, respectively.

For this ideal model, it is straightforward to determine the voltage between the output terminal x and terminal $x2$ In the general analysis presented earlier, x represents a phase, and the phase may be a, b, or c. Each leg of the H-bridge has a voltage-clamping capacitor, and the voltages at the two input terminals of the reactor can be 0, $v_{dc}/2$, or v_{dc} , where

$v_{dc}$is the nominal voltage of the capacitorC_{dc}, as shown inFig. 1. For each phase, there are nine different switching states, corresponding to nine terminal voltage combinations. These combinations can produce a line-to-ground voltage at the output terminal that has seven distinct voltage levels. For phase *a*, these states are detailed in Table I.

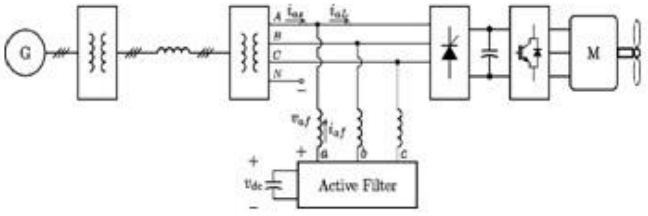

Fig.3 Active filter connection to a shipboard powersystem.

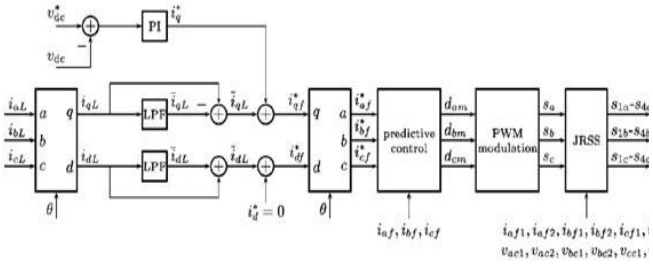

Fig. 4.Active filter control diagram.

In Table I, *Sa*is the switching state that is defined as being 0 for the lowest possible line-to-ground voltage. The voltages *Va*1 and *Va*2 are the line-to-ground voltages applied to the left and right side of the reactor in Fig. 1, respectively. The voltage *Vag*is as defined in Fig. 1 and calculated using (2). Note that there are two redundant states 2′and 4′that produce the same voltage as states 2 and 4, respectively. However, these are not desirable, and will be ignored, because the voltages applied across the reactor are twice as high as the other states. The output current for each phase is split between the two legs of the H-bridge structure. Ideally, two-thirds of the current will come from *X*1 and one-third from *X*2 so that the magnetizing current is zero. The control given later discusses the regulation of the reactor currents so as to minimize the magnetizing current.

B. Active Filter Interface

As shown in Fig. 3, the active filter is connected to the power system via a three-phase inductor L_f . The filtering function is achieved by injecting a compensating harmonic current into the point of common coupling of the utility–load interface, which in this case is the secondary side of the rectifier load trans-former. The reference harmonic currents are extracted from the load currents so that the sum of the load currents and the injection currents has a THD that meets required specifications. The seven-level inverter can produce an output voltage that contains much less switching frequency ripple than a conventional two-level inverter; thus, the generated injection currents are smoother and the.

According to the inverter equations, the line-to-neutral volt-age v_{af} depicted in Fig. 3 can be related to the inverter line-to-ground voltages. Having established the model for the proposed active filter, the following section describes the details of the control.

III. Active Filter Control:

To effectively compensate the load harmonic currents, the active filter controller should be designed to meet the following three goals:

1) extract and inject load harmonic currents;

2) maintain a constant dc capacitor voltage;

3) avoid generating or absorbing reactive power with funda-mental frequency components.

A. Harmonic Current Extraction

For diode or thyristor rectifier loads, the most common har-monic currents are of the 5th, 7th, 11th, and 13th order. Although a high-pass filter can be used to extract these components di-rectly from the line currents, it is not feasible to obtain high attenuation at the fundamental frequency due to the high cur-rent amplitude. The synchronous *q–d* reference frame controller developed for shunt active filter systems is used to generate the reference compensating current [2]. As shown in Fig. 4, the mea-sured load phase currents (i_{aL},i_{bL} , and i_{cL}) are first transformed into the synchronous reference frame to obtain i_{qL} and i_{dL}. The synchronous reference frame phase angle can be obtained by processing the measured system voltage with a phase-locked loop circuit or algorithm. Low-pass filters are then used to ex-tract the dc components, which correspond to the fundamental frequency components of the load currents. The dc component is removed by a simple subtraction of the filtered components

(i_{qL} andi_{dL}) and the transformed components (i_{qL} and i_{dL}).

B. DC Capacitor Voltage Control

For the active filter to operate effectively, it is important to maintain the dc capacitor voltage at a constant value. Since the active filter topology is essentially identical to that of an active

rectifier, similar control strategies for the active rectifier are applicable.

The dc capacitor voltage is directly affected by the real power transferred across the active filter. To keep the voltage con-stant, ideally, no real power should be transferred. However, due to losses in switching devices and other components, a small amount of real power is needed. In the synchronous reference frame with the *q*-axis aligned with the voltage at the point of common coupling, the real power transferred can be expressed as

$$P = \frac{3}{2} v_q i_{qf} \quad (4)$$

which means that by adjusting the *q*-axis filter current, the real power can be effectively controlled. The capacitor voltage reg-ulation is then handled by a simple proportional-integral (PI) control adding to the *q*-axis filter current, as shown in Fig. 4.

C. Reactive Power Control

In most cases, a unity power factor for fundamental frequency components is required at the active filter terminals. Since the reactive power can be expressed as

$$Q = \frac{3}{2} v_q i_{df} \quad (5)$$

this goal can be achieved by keeping the average *d*-axis current at zero, as shown in Fig. 4. The combined control of dc capacitor voltage and reactive power uniquely determines the fundamental frequency component of the active filter output current. This current is then superimposed onto the commanded harmonic currents, and the commanded filter currents i^*_{af} ,i^*_{bf} , and i^*_{cf} are obtained by the reverse transformation, as shown in Fig. 4.

D. Harmonic Current Regulator

A current regulator is needed to generate the commanded compensation current. Generally, a hysteresis control provides fast response and is suitable for nonsinusoidal current track-ing. However, it suffers from some serious disadvantages such as variable switching frequency and phase interaction prob-lems [1]. In addition, to fully take advantage of the benefits of a multilevel converter, a current regulator that uses a voltage-source pulsewidth modulation (PWM) is desirable. Several frequency-selective harmonic current regulators were proposed in [14]–[17] that achieve zero steady-state error for the dom-inant harmonics. Nonetheless, they all have to target specific frequencies and require a significant amount of computation time.

In this paper, a predictive current regulator is implemented to track the harmonic currents, which has the advantages of simple structure and less computational requirement. Given the mea-sured system voltages and filter inductor currents, the required phase *a* filter voltage can be calculated based on the known value of the filter inductance

$$v_{af}' = \hat{v}_{as} + \frac{(\hat{i}'_{af} - i_{af})L_f}{\Delta t} \quad (6)$$

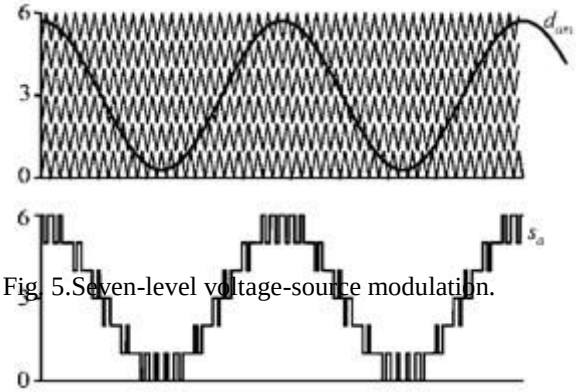

Fig. 5.Seven-level voltage-source modulation.

where Δt is the controller switching period, $\hat{v}_{as}$ is the pre-dicted source voltage and can be calculated through linear extrapolation

$$\hat{v}_{as} = v_{as}(t) + 1.5\Delta t\ [v_{as}(t) - v_{as}(t - \Delta t)] \quad (7)$$

and $\hat{i}'_{af}$ is the predicted reference harmonic current

$$\hat{i}'_{af} = i'_{af}(t) + 2\Delta t\ [i'_{af}(t) - i'_{af}(t - \Delta t)]. \quad (8)$$

For accurate current tracking, the prediction takes into account the controller delay due to data acquisition and calculation. Better performance has been achieved when a second-order prediction method is used.

As can be seen, the predictive control effectively turns the commanded currents into commanded voltages suitable for a voltage-source modulator. These commanded voltages are then expressed as PWM duty cycles by normalizing them to the dc voltage and giving them an appropriate range. For phase *a*, the duty cycle can be expressed as

$$d_{am} = \frac{3v_{af}}{v_{dc}} + 0.5 \quad (n - 1) \quad (9)$$

where*n* is the number of voltage levels, which for this topology is $n = 7$. Similar expressions can be written for phase *b* and phase *c*. The predictive control is shown in Fig. 4 having outputs to the PWM modulator

E. Multilevel Voltage-Source Modulation

The seven-level voltage-source modulation is accomplished by comparing the duty cycles with a set of six carrier waveforms. This is illustrated for phase *a* in Fig. 5. The resulting switching state s_a is the number of triangle waveforms that the duty cycle is greater than. Therefore, the switching state has a range of 0–6, and this is in agreement with Table I.

F. Capacitor Voltage Balancing

After carrying out the modulation, the switching states for each phase need to be broken out into transistor signals. In order to have the correct voltage levels, the flying capacitors must remain charged at exactly $v_{dc}/2$. This can easily be assured using the redundancy of the inverter legs.

IV. Simulation Results:

Numerical simulations have been conducted in the Advanced Continuous Simulation Language (ACSL) to validate the proposed topology. The example naval ship power system has a rated line-to-line voltage of 4.16 kV and a three-phase six-pulse diode rectifier. A three-phase PWM inverter is connected to the rectifier dc bus, and supplies power to a permanent-magnet synchronous motor load. The rated dc capacitor voltage of the active filter is 6800 V. The three-phase tapped reactor has a leakage inductance of L_l= 50 μH, winding resistance r = 0.1 Ω, and mutual inductance L_M = 1 H. The active filter interface inductance is L_f = 0.1 mH.

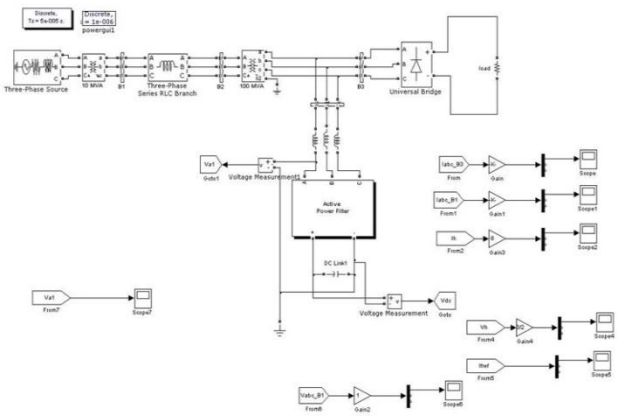

Fig: Seven-level Shunt Active filter Simulation Diagram

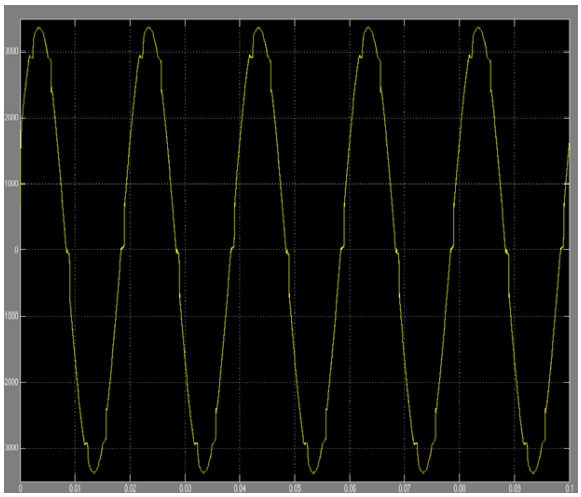

Fig :Line to Neutral Voltage Waveform

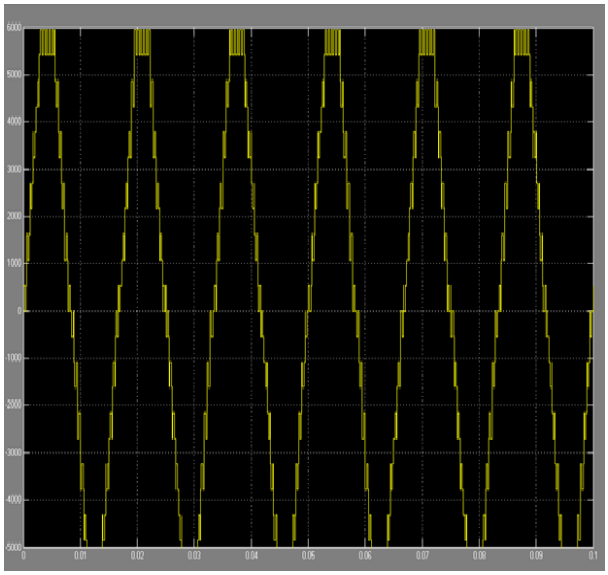

Fig :Reactor terminal output Voltage Waveform

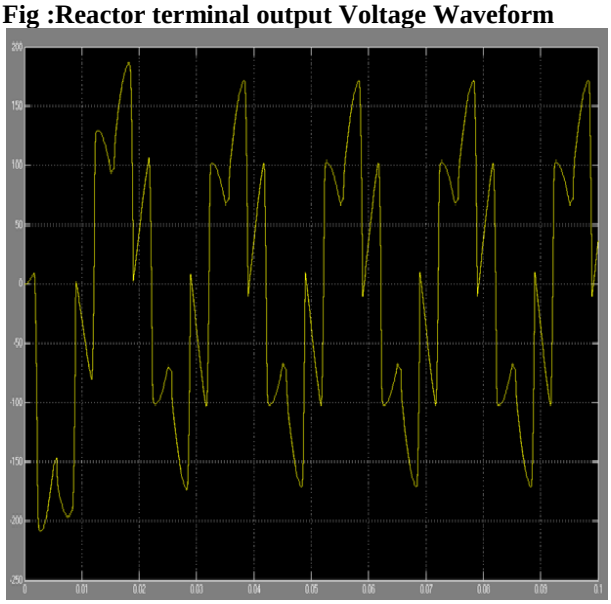

Fig : compensated source current waveform

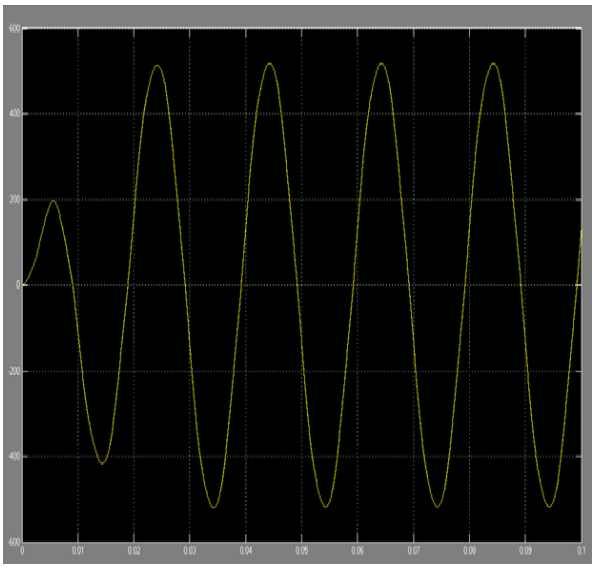

Fig :Source Harmonic Current Waveform

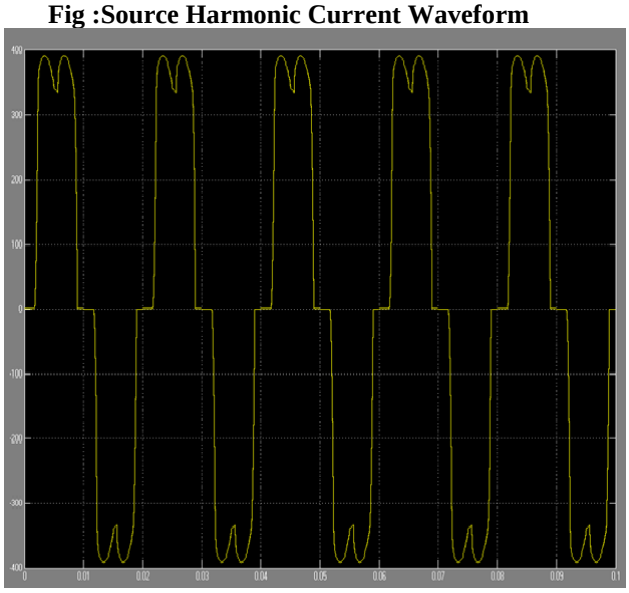

Fig :Load Harmonic Current Waveform

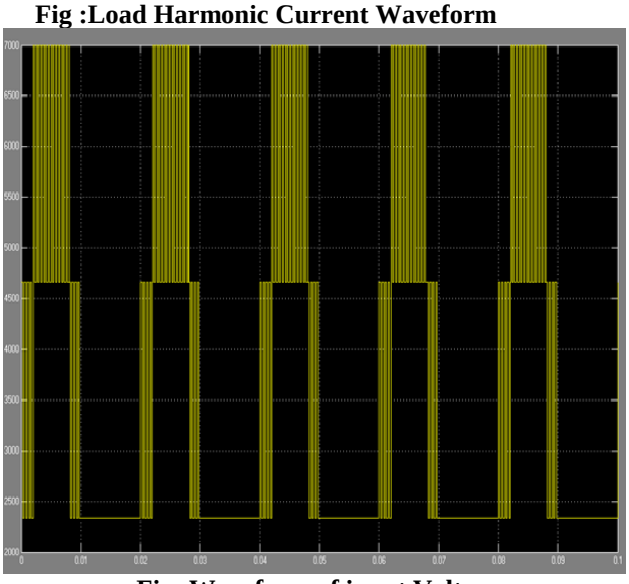

Fig :Waveform of input Voltage

V. Conclusion:

A new type of power converter has been introduced in this paper. The converter is based on parallel connection of phase legs through an interphase reactor. However, the reactor has an off-center tap at one-third resulting in an increased number of voltage levels. Specifically, two three-level flying capacitor phase legs are paralleled in this way to form a seven-level power converter. The converter is utilized in an active filter application. The details of the high-level control as well as the switching control have been presented. The control ensures reactor current sharing as well as flying capacitor voltage balance. The proposed active filter has been validated for a naval ship board power system using detailed simulation and RTDS hardware.

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